ESCUELA SUPERIOR POLITÉCNICA DEL LITORAL
Faculty of Electrical and Computer Engineering
COURSE SYLLABUS
Digital Systems I

1. CODE AND NUMBER OF CREDITS

CODE	FIEC00299	
NUMBER OF CREDITS: 4	**Theoretical: 4**	**Practical: 0**

2. COURSE DESCRIPTION

The Digital Systems I course introduces the basic concepts for the design, construction and analysis of circuits digital electronics. Initially studying binary numbers, codes and their applications, then present the other basic components and then scaling elements integration required for the construction of Digital Systems. Additionally, the basic concepts of sequential circuits. The implementation systems is studied with traditional discrete elements and the aid of hardware description language VHDL.

3. PRE-REQUISITES AND CO-REQUISITES

PRE-REQUISITES	FIEC01735 ELECTRICAL NETWORK ANALYSIS I
CO-REQUISITES	

4. CORE TEXT AND OTHER REQUIRED REFERENCES FOR THE TEACHING OF THE COURSE

CORE TEXT	1. Brown S., Vranesic Z., Fundamentals of Digital Logic with VHDL Design, Second edition, 2006, McGraw Hill.
REFERENCES	1. Wakerley J., Digital Design, Principles and Practices, 2001, McGraw Hill, 2. Perez S. y Soto E., Diseño de Sistemas Digitales con VHDL, 2002, Thomson. 3. Villar E. y otros, VHDL Lenguaje estándar de diseño electrónico, 1998, McGraw Hill. 4. Mandado E. y otros, Dispositivos Lógicos Programables y sus Aplicaciones, 2002, Thomson. 5. Fletcher W., An Engineering Approach to Digital Design. 6. Tocci R., Sistemas Digitales, Principios y Aplicaciones, Prentice Hall, 2001. 7. Hernández A., Introducción al Diseño Digital de Circuitos Combinacionales y secuenciales, 2002, CIME, ISPJAE. 8. Blanco N. y Carlos J., Libros Electrónicos para la Enseñanza de los Circuitos Lógicos, versión 2.1, 2003.

5. COURSE LEARNING OUTCOMES

At the end of the course, the student will be able to:
1. Design and implement combinatorial logic circuits.
2. Use integrated circuit SSI, MSI and LSI to implement combinational circuits.
3. Use a hardware description language such as VHDL in the description and simulation of the combinatorial logic circuits.

6. COURSE PROGRAM

I. NUMERICAL SYSTEMS AND CODES. (4 sessions - 8 hours).
- Binary, octal and hexadecimal numerical Systems.
- Conversion of numerical systems.
- Sum and subtraction of non-decimal numbers.
- Representation negative numbers.
- Complements numbers. Multiplication and binary division.
- Binary Codes of numbers. Gray Code. Character codes. Error detection codes. Code for transmission and storage of serial data.

II. COMBINATORIAL LOGIC DESIGN PRINCIPLES. (7 sessions - 14 hours).

- Truth Tables. Basic logic gates. Gates universal equivalences.
- The switching algebra as a basic tool for working with logic circuits. Postulates and theorems.
- Representation logic functions by sum of products and sums products.
- Minterms and maxterms. Combinations do not care.
- Minimization logic functions. Methods Karnaugh maps. Analysis and synthesis of logic functions.
- General synthesis method using logic gates.

III. HARDWARE DESCRIPTION LANGUAGE VHDL (3 sessions - 6 hours).
- Entity and architecture.
- Data types, signals and variable.
- Operators. Syntax.
- Structural descriptions by data flow and behaviors. Concurrent and sequential VHDL.
- Hierarchical design. Packages and libraries.
- Simulations using the software Max + PlusII, Altera.

IV. LOGIC FAMILIES (2 sessions - 4 hours).
- Logic families CMOS and TTL
- Analysis of the principal characteristics of CMOS and TTL series
- Interface between the two families.

V. MSI INTEGRATED CIRCUITS AND APPLICATIONS IN COMBINATORIAL LOGIC DESIGN. (7 sessions – 14 hours).
- Arithmetic circuits: full adder, n-bit parallel adder with serial transmission.
- Comparators, Multiplexers, Decoders: binary decoders of n-a-2^n decoder driver
- Coders: code converters, coders of priority.
- Description of these circuits with VHDL.
- Analysis and design of combinatorial circuit using integrated circuits of medium scale of integration.
- Design with decoders and multiplexers.
- Connection to basic input / output devices such as switches and LEDs.

VI. PRINCIPLES OF SEQUENTIAL LOGIC DESIGN. (4 sessions - 8 hours).
- Basic binary cell, RS flip-flops, D, T and JK.
- Triggered by flank or enabling by level, master-slave operation.
- Shift registers, synchronous and asynchronous binary counters, other types of counters: Ring and Johnson.
- Description VHDL.

VII. LARGE SCALE INTEGRATED CIRCUITS LSI, SPLD AND ITS APPLICATIONS. (1 session - two hours).
- ROM, PROM, EPROM, EEPROM and Flash Memories.
- Programmable devices PAL and PLA.
- Applications the design of combinatorial logic.

7. WORKLOAD: THEORY/PRACTICE

Two class sessions per week, two hours each.

8. CONTRIBUTION OF THE COURSE TO THE EDUCATION OF THE STUDENT

The Digital Systems I course is oriented to engineering design

BASIC TRAINING	PROFESSIONAL TRAINING	SOCIAL SKILLS DEVELOPMENT
	X	

9. THE RELATIONSHIP BETWEEN THE LEARNING OUTCOMES OF THE COURSE AND THE LEARNING OUTCOMES OF THE DEGREE PROGRAM

LEARNING OUTCOMES OF THE DEGREE PROGRAM*	CONTRIBUTION (High, Medium, Low)	LEARNING OUTCOMES OF THE COURSE**	THE STUDENT MUST:
a) An ability to apply knowledge of mathematics, science and engineering.	Medium	2	Apply the knowledge acquired in electrical network courses and logical mathematics.
b) An ability to design and conduct experiments, and to analyze and interpret data	Low		Able to analyze the results of the simulation of Digital systems designs

c)	An ability to design a system, component or process to satisfy realistic constraints.	High	1	Design various combinatorial circuits based on truth tables or simple architectures.
d)	An ability to function on multidisciplinary teams.	---		
e)	An ability to identify, formulate and solve engineering problems.	Low		Solve basic digital design problems.
f)	An understanding of ethical and professional responsibility.	Low		
g)	An ability to communicate effectively.	Low		To know to defend and support a finding of design used in lessons and exams.
h)	A broad education necessary to understand the impact of engineering solutions in a social, environmental, economic and global context.	Low		
i)	A recognition of the need for, and an ability to engage in life-long learning.	Medium	2	To be prepared to design using basic languages that can change in the medium term.
j)	A knowledge of contemporary issues.	High	2	Understand the operation and programming of modern chips.
k)	An ability to use the techniques, skills, and modern tools necessary for engineering practice.	Medium	3	To drive simulators and virtual laboratory equipment.
l)	Capacity to lead, manage and undertake projects.	---		

10. EVALUATION IN THE COURSE

Evaluation activities	
Exams	**X**
Tests	**X**
Homework/tasks	**X**
Projects	
Laboratory/Experiments	
Class participation	
Visits	
Other	

11. PERSON RESPONSIBLE FOR THE CREATION OF THE SYLLABUS AND THE DATE OF ITS CREATION

Created by	Eng. Sara Ríos
Date	April 21, 2013

12. APPROVAL

ACADEMIC SECRETARY OF THE ACADEMIC DEPARTMENT	DIRECTOR OF TECHNICAL ACADEMIC SECRETARY
NAME: Mrs. Leonor Caicedo G.	NAME: Eng. Marcos Mendoza
SIGNATURE:	SIGNATURE:
Date of approval by the Directive Council: 2013-537 2013-10-7	

ESCUELA SUPERIOR POLITÉCNICA DEL LITORAL
Ing. Marcos Mendoza V.
DIRECTOR DE LA SECRETARÍA TÉCNICA ACADÉMICA

13. VALIDITY OF THE SYLLABUS

RESOLUTION OF THE POLYTECHNIC BOARD:	13-12-343
DATE:	2013-12-12